LECTURE 10

Computer Architecture
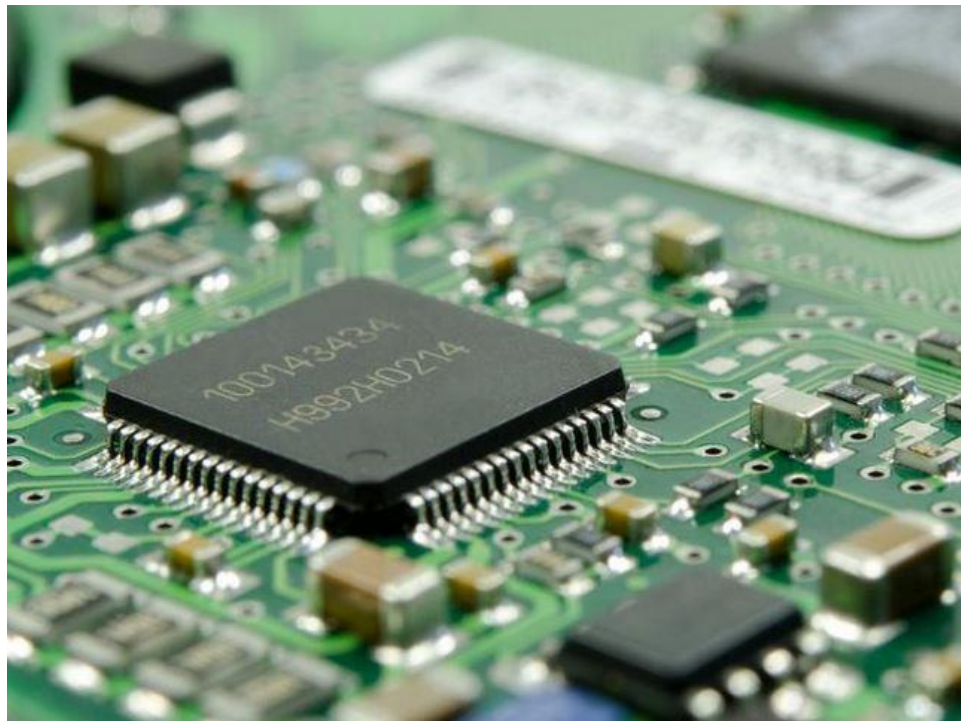
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Performance of Cache Memory

1. Average Cost (معدل الكلفة)

(Measurement of Cache memory performance) ويستخدم لقياس اداء الذاكرة

$$Cs = \frac{CcSc + CmSm}{Sc + Sm}$$

حيث ان :

C_s: Average cost of system per byte , (main memory plus cache)

C_c: Average cost of cache

C_m: Average cost of main

S_c: Size of cache memory

S_m: Size of main memory

2. System Access Time

$$T_s = HTc + MT_m$$

M=(1- H) :حيث ان

T_s: Average system access time

T_c: cache access time

H: hit ratio

M: Miss ratio

T_m: main access time

Example(1): Assume Tc=100 ns , Tm=1000 ns and H=0.9, find Ts?

Solution)

$T_s = HT_c + (1-H)T_m$

$T_s = 0.9 * 100 + (1-0.9)*1000$

$T_s = 190\ ns$

Example(2): Assume Tc=150 ns , Tm=1500 ns and Ts=250 ns, find H?

Solution)

$T_s = HT_c + MT_m$

$T_s = HT_c + (1-H)T_m$

$T_s = HT_c + Tm - HT_m$

$T_s - T_m = H(T_c - T_m)$

$$H = \frac{Ts - Tm}{Tc - TM}$$

$$H = \frac{250 - 1500}{150 - 1500}$$

$$H = \frac{-1250}{-1350}$$

$H = 0.92$ *this computer is perfect*

Example(3): Assume Tc=0.000000175 s , Tm=900 ns and H=0.7,

find Ts?

Solution:

$$T_s = HT_c + (1-H)T_m$$

$$T_s = 0.7 * 175*10^{-9} + (1-0.7)*900$$

$$T_s = 392.5 \ ns$$

Example(4): Assume Tc=300 sec , Tm=1800 sec and Ts=1450 sec, find Hit ratio?

Solution)

$$T_s = HT_c + MT_m$$

$$T_s = HT_c + (1-H)T_m$$

$$T_s = HT_c + T_m - HT_m$$

$$T_s - T_m = H(T_c - T_m)$$

$$H = \frac{Ts - Tm}{Tc - Tm}$$

$$H = \frac{1450 - 1800}{300 - 1800}$$

$$H = \frac{-350}{-500}$$

$$H = 0.7 \ this \ computer \ isn't \ perfect$$

نلاحظ من خلال المثال (2) والمثال (4) انه كلما كان زمن الوصول للمعلومة في الكاش (Tc) سريع كلما كان الـ Hit ratio قريب من الواحد وكانت فرصة العثور على المعلومة اكبر وكانت الحاسبة مثالية perfect .

Cache Mapping

❖ **Elements of Cache Design**

- —cache Size

- —Mapping Technique

    direct, associative, set associative

- —Replacement Algorithm

    LRU, FIFO, LFU, Random

- —Write Policy

    Write through, Write back

- —Number of Caches

   single or two level

- **Mapping Technique**

The transformation of data from main memory to cache memory is referred to as a mapping process.

Cache Memory Mapping: It means how the main memory data will get mapped into the cache memory, it is copy not moved.

الـ Cache Memory Mapping هي تقنية او الية ينفذها نظام التشغيل لارسال نسخة من البيانات المخزونة داخل الـ main memory عن طريق ارسال وتحديد الـ Block القادم من الـ main memory في اي slot داخل الـ cache سوف يخزن وذلك لكي تكون عملية البحث عن المعلومة داخل الـ cache من قبل المعالج تكون منظمة وسهلة.

- **Cache Mapping Techniques**

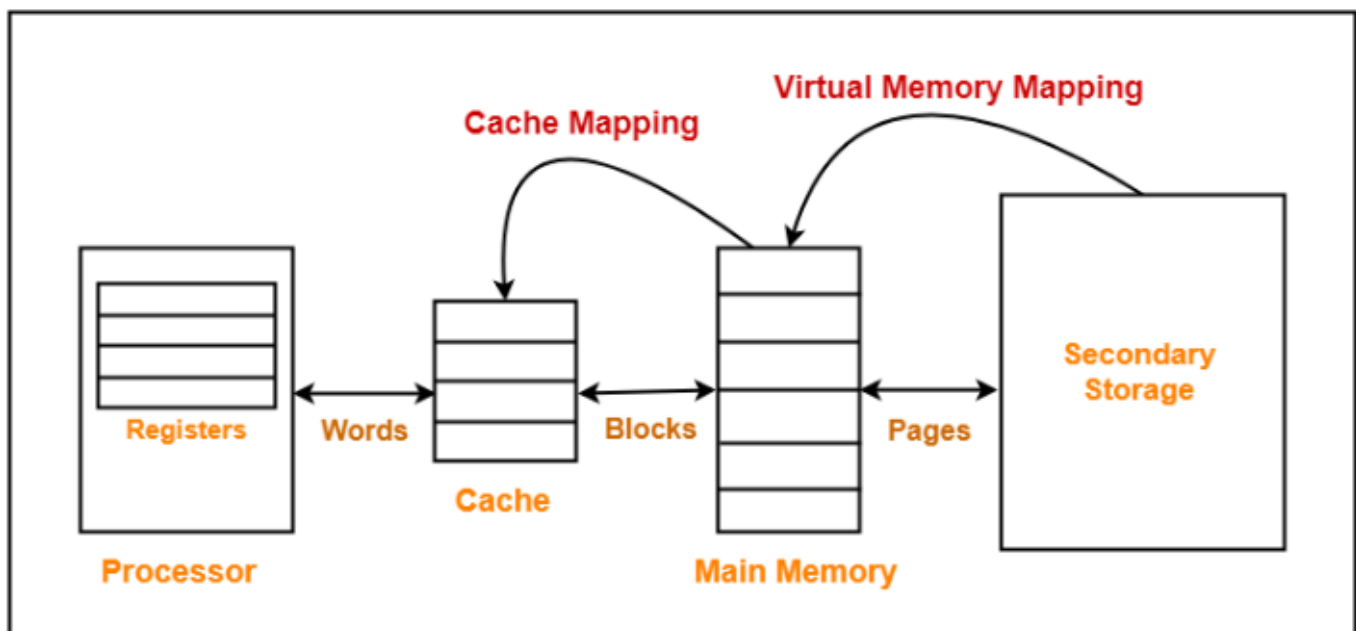Cache mapping is performed using following three different techniques:
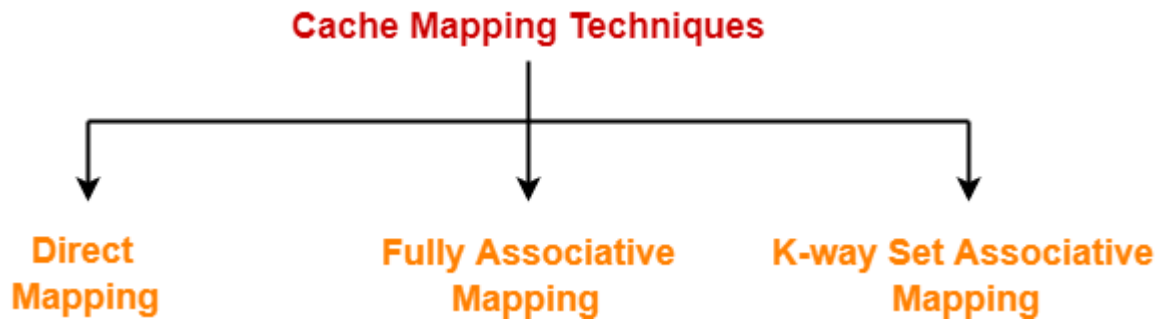
1-**Associative mapping**

2-**Direct mapping**

3-**Set-associative mapping**

The following diagram illustrates the mapping process:

Block diagram illustrate cache mapping

NOTES

- Main memory is divided into equal size partitions called as **blocks** .

- Cache memory is divided into partitions having same size as that of blocks called as **lines** or **slot**.

- During cache mapping, block of main memory is simply copied to the cache.

يتم حساب عدد الـ blocks الموجودة في الـ main memory بأستخدام القانون التالي:

1. *No. of block in main memory* $= \dfrac{size\ of\ memory}{size\ of\ block} = \dfrac{Sm}{Sblock}$

يتم حساب عدد الـ slots الموجودة في الـ cache memory بأستخدام القانون التالي:

2. *No. of block in cache memory* $= \dfrac{size\ of\ cache}{size\ of\ slot} = \dfrac{Sc}{Sblock}$

يتم حساب no. of address bus عن طريق حجم الذاكرة memory size:

3. *Size of memory* $= 2^{no.of\ address\ bus}$

Example(1) : Suppose cache size= 4K byte, memory size= 32kbyte, data is to be transferred between main memory and cache in blocks of 16 bytes. Find:

1. No. of block in main memory

2. No. of block in cache memory

3. No. of address bus

Solution)

1. *No. of block in main memory* $= \dfrac{size\ of\ memory}{size\ of\ block} = \dfrac{32k}{16} = 2^{15}/\,2^{4}$

$=2^{11}=2k$

2. *No. of block in cache memory* $= \dfrac{size\ of\ cache}{size\ of\ slot} = \dfrac{4k}{16} = 2^{12}/2^{4} = 2^{8} = 256$

3. *Size of memory* $= 2^{no.of\ address\ bus} = 32k = 2^{15}$

No. of address bus = 15

Example(2): Suppose cache size= IK byte, memory size= 64kbyte, data is to be transferred between main memory and cache in blocks of 8 bytes. Find:

1. No. of block in main memory

2. No. of block in cache memory

3. No. of address bus

Solution)

1. *No. of block in block memory* $= \dfrac{size\ of\ memory}{size\ of\ block} = \dfrac{64k}{8} = 2^{16}/2^{3}=2^{13}=8k$

2. *No. of block in cache memory* $= \dfrac{size\ of\ cache}{size\ of\ slot} = \dfrac{1k}{8} =2^{10}/2^{3}=2^{7}=128$

3. *Size of memory* $= 2^{no.of\ address\ bus} = 64k =2^{16}$

No. of address bus = 16